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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/868,048	07/16/2001	Mana Hamada	HYAE:120	5497

7590 06/09/2004

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	10

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/868,048	HAMADA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 4* is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4 are presented for examination.

2. Claim 2 is objected to because of the following informalities: "said step" in line 6. Appropriate correction is required. It is understood that the "said step" in line 6 is referring to source data supply processing step (line 3) in parallel with the state flag processing step . Examiner believes that it is directed to minor language formality, therefore, applicant is suggested to provide correction in the next response.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (5,617,486) in view of Vassiliadis et al. (4,924,422).

4. As to claims 1, 3, Chow disclosed a vector processing system comprising at least :

a) an arithmetic decision step (see fig.9) for computing (see fig.8 [84] and deciding (see fig.883], fig.9 [92]) an arithmetic operation was to perform when target data [M vectors] was obtained (see col.13, lines 34-39;

b) an arithmetic control, step to execute vector arithmetic for the target data [a] and output the result (see the corrected r' in col.13, lines 40-49, lines 55-60, see the

arithmetic vector calculation in col.14, lines 21-65), or output the target data (see more M accumulation vector data being collected or accessed in col.13, lines 50-55, see the factored in vector in col.14, lines 1-9, see only the calculation of the corrected vector until the M vectors reached).

5. Chow did not specifically teach the computing and the decision are processed in parallel as claimed. However, Vassiliadis disclosed an arithmetic system for computing an arithmetic result [RESULT] by an arithmetic operation unit [10] in parallel with a decision step performed by a determination circuit [25] to predict the arithmetic result and therefore, reducing the delay (e.g. col.2, lines 55-62, col.3, lines 61-68, col.4, lines 1-4, see the decision was made in col.5, lines 1-15, col.9, lines 26-33). It would have been obvious to one of ordinary skill in the art to use Vassiliadis in Chow for computing and deciding the vector arithmetic in parallel as claimed because the use of Vassiliadis could provide Chow the processing capability to accept the input vector data concurrently with the decision for processing, thereby minimizing the wait cycle by the subsequent operation , and it could be readily achieved by configuring the parallel computing and decision circuits of Vassiliadis into Chow with modified control parameters, such as the read and write commands, recognizable by Chow, in order to enhance the processing bandwidth, and because Vassiliadis showed the parallel computing and decision was applicable in a vector arithmetic processing unit (see the array of input operands px +py in col.7, lies 15-25), for the above reasons, provided a motivation. Chow is used as primary reference because it showed the detailed

computing and decision features. Vassiliadis is used as secondary because it showed the implementation of the arithemtic computation in parallel with a decision step.

6. Claim 2 is allowable over the art of record for reciting the combined features of the first stage of parallel retaining state flag, the sequentially retaining state of he data, and the second stage of making the condition of decision in parallel, the third stage for successive storage of the arithmetic results and the output of data supplied to the prescribed source among the data which are supplied as the arithmetic result when condition is not satisfied.

7. Claim 4 is allowable over the art of record for reciting the combined features of the first N registers and the pipeline register, the arithmetic result means for storing the result, the condition decision means for indicating satisfied condition based on the state flag and condition specified by vector arithmetic instruction, and the execution of the vector instruction by the pipeline of the first stage with the storage of the source data in parallel with the state flag, and the second stage of the processing the result of the N registers to the pipeline register in parallel with the condition outputs, and the selection mode.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Booth (5,247,696) is cited for the background teaching of the vector sum of the operand input data (e.g. see col.2, lines 23-45, see also the conditional decision in col.7, lines 53-68, col.8, lines 1-31).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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